Cptr350 **Exam #1** **2015**

NAME KEY SCORE 50 (50)

This is a closed book test. Reference materials allowed are both sides of an 8.5"x11" sheet and your calculator. Unless otherwise noted, all questions relate to the MIPS processor and its instruction set. Please turn in all your work done on this exam except for your cheat sheet.

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4 pts For the binary numbers represented in ***two's complement*** form:
1) Do the operation as an ALU math unit would do it and indicate the binary result.
2) Was the Carry Flag set during the operation?
3) Does this condition of the Carry Flag indicate a correct or incorrect result?

```
  10111000     -72
+ 01101100   + 108
-----------  -----
  00100100     +36
```

Carry Set

Correct Result

```
  10111000     -72
- 01101100   -(+108)
-----------  ------
                -180   <- OUT of Range
```

```
  10111000
+ 10010011
+        1
----------
  01001100
```

Carry = 1

Incorrect Result

1000 0001 1110 0000 0000 0000 0000 0000

4 pts The 32-bit binary pattern shown above is in ***floating-point number*** format. What is the equivalent decimal number that it represents?

Sign Bit = 1 = Negative

Biased exp = 0000 0011

Real exp = $3 - 127 = -124_2$

mantissa = 1.1100....

Number = $-(1.11e^{-124})_2 = -8.2285 \times 10^{-38}$

5 pts Show the IEEE754 32-bit floating point representation of the decimal number 60.625

$60.625 = 111100.101_2$

$= 1.11100101\ e^5$

sign bit = 0 = positive

biased exp = $5 + 127 = 132 = 10000100_2$

mantissa = 1.11100101

0 | 10000100 | 11100101000....

The following true/false problems are worth one point each. Circle the correct answer.

T (F) The performance metric called MIPS is constant between different programs run on the same computer.

(T) F System performance is the reciprocal of execution time.

(T) F Subtraction of two's complement numbers can be performed with an adder circuit if the number to be subtracted is first complemented and the carry-in to the LSB of the adder is asserted.

T (F) The radix-4 Booth multiplication algorithm cannot be used accurately on two's complement numbers.

T (F) When comparing CPU's, the one with the highest clock rate has the highest performance.

(T) F The opcode field of a MIPS instruction is 6-bits long.

(T) F The decimal number -1.25_{10} can be represented ***exactly*** in IEEE754 floating-point format.

T (F) In the MIPS 5-stage pipeline, all structural hazards can be eliminated through data forwarding.

(T) F Four pipeline registers are required for a five-stage pipeline.

T (F) Pipelining increases overall throughput by reducing single instruction latency.

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2 pts What does it mean to "sign-extend" a register?

1 pt Typical pipelined data path implementations use 5 steps. What is the correct ordering of these steps? (Circle the correct response)

a – memory access, instruction fetch, decode, execute, write back
b – instruction fetch, decode, memory access, execute, write back
c – instruction fetch, execute, decode, memory access, write back
d – depends on the instruction
(e) – none of the above

2 pts In the snippet of MIPS assembly code below, how many times is instruction memory accessed? How many times is data memory accessed? Count only accesses to memory, not registers.

```
lw $v1, 0($a0)
addi $v0, $v0, 1
sw $v1, 0($a1)
addi $a0, $a0, 1
```

Instruction Memory 4 Data Memory 2

You are part of a computer design team that has recently completed the architectural design and compiler for a new computer. The plan is to use a 1GHz clock. The following have been determined from simulation:

Instruction Class	CPI	Frequency
A	2	30%
B	3	30%
C	3	25%
D	5	15%

Show all work for the problems below.

3 pts Find the CPI for the machine.

$2(.3) + 3(.3) + 3(.25) + 5(.15) = 3.0$

3 pts What is the MIPS rating for this computer?

$$\frac{1 \times 10^9 \text{ cycles/sec}}{3.0 \text{ cycles/INST}} = 333 \text{ MIPS}$$

3 pts What change in performance would result if the CPI for instruction class D decreased from 5 to 4 but a 5% slower clock would also be required?

New CPI : $(2)(.3) + 3(.3) + 3(.25) + 4(.15) = 2.95$

New MIPS: $\frac{.95 \times 10^9}{2.95} = 333 \text{ MIPS}$

no change

3 pts Suppose that a clever member of your design team discovers how to reduce the CPI of any one instruction class by one cycle without affecting the CPU clock rate (i.e. you can pick one of the four classes to be reduced by one clock period). Which instruction class would you choose? Why?

A: $1(.3) + 3(.3) + 3(.25) + 5(.15) = 2.7$

B: $2(.3) + 2(.3) + 3(.25) + 5(.15) = 2.7$

} either one - results in most performance

C: $2(.3) + 3(.3) + 2(.25) + 5(.15) = 2.75$

D: $2(.3) + 3(.3) + 3(.3) + 4(.15) = 2.85$

10 pts Using the Booth radix-4 multiplication algorithm show in longhand the multiplication of the two 4-bit decimal numbers: -2_{10} (1110_2) and $+3_{10}$ (0011_2). You may use the radix-2 method for 80% credit.

b = -2 = 1110 a = 0011

2b = -4 = 1100

-b = 2 = 0010

-2b = 4 = 0100

RESULT = -6 = 1010

000	Do nothing
001	+b
010	+b
011	+2b
100	-2b
101	-b
110	-b
111	Do nothing

```
  0000 0011 0      a00 - b
+ 0010
  0010 0011        SHIFT #1
  0000 1000 1
+ 1110             ADD +b
  1110 1000
  1111 1010        SHIFT #2
```

ANSWER = $1111\ 1010_2 = -6_{10}$

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b = 3 = 0011 a = -2 = 1110

2b = 6 = 0110

-b = -3 = 1101

-2b = -6 = 1010

```
  0000 1110 0      a00 - 2b
+ 1010
  1010 1110
  1110 1011 1      SHIFT #1
                   DO NOTHING
  1111 1010        SHIFT #2
```

ANSWER = $1111\ 1010_2 = -6_{10}$